Please add the following claims:

A method of providing operational power to a portable utilization device, said method comprising:

- (a) storing in an electronic memory device contained within a battery pack, battery pack data related to battery pack characteristics;
 - (b) coupling the battery pack with the portable utilization device;
 - (c) monitoring present battery pack conditions;
 - (d) retrieving the battery pack data;
- (e) communicating information based on the present battery pack conditions and based on the battery pack data to processing circuitry of the portable utilization device; and
- (f) controlling the utilization of the battery pack by said portable utilization device.--

A method of providing operational power to a portable utilization device, said method comprising:

- (a) coupling a battery pack with an electronic memory system and with processing circuitry of the portable utilization device;
- (b) incorporating in the electronic memory system, battery pack data related to battery pack characteristics of the battery pack;
 - (c) monitoring present battery pack conditions;

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- (d) retrieving the battery pack data;
- (e) communicating information based on the present battery pack conditions and based on the battery pack data to processing circuitry of the portable utilization device; and
- (f) controlling the utilization of the battery pack by said portable utilization device.--
- --13. A method according to Claim 12, wherein the processing circuitry is responsive to a low power condition of the portable utilization device to conserve power.--
- --14. A method according to Claim 12, wherein in response to a low power condition, the portable utilization device is placed in a powered down mode without loss of data.--
- --15. A method according to Claim 12, wherein the processing circuitry is operative to monitor power consumed by various components associated with the portable utilization device.--
- --16. A method according to Claim 12, wherein the portable utilization device controls clock operating speed of the processing circuitry to reduce power

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